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09/615,705	07/13/2000	Yoko Horiguchi	Q60098	4487

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/615,705	Applicant(s) HORIGUCHI, YOKO	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15,17-19 and 21-32* is/are pending in the application.

4a) Of the above claim(s) *2,4-7,9,11,15,17-19,24 and 30-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8,10,12,13,21-23 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The corrected or substitute drawings were received on 6/13/2002. These drawings are approved by the examiner.

Election/Restriction

2. Claims 30-32 are withdrawn from consideration pursuant to 37 CFR 1.142(b), as being drawn to nonelected embodiments. Applicant elected in paper 5 the embodiment of figure 1. The claimed limitations of claims 30-32 are not recited in the written description of the first embodiment, but rather in the description of the embodiments of figures 4-14. Even applicant admits that the claimed limitations of claims 30-32, which recite similar subject matter as claims 27-29 (page 7 of applicant's arguments) are described in the embodiments of figures 4-14 (page 6 of applicant's arguments). Therefore, claims 30-32 are withdrawn from consideration.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 27-29 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the

application was filed, had possession of the claimed invention. There is no adequate description in the disclosure of the embodiment of figure 1 for an ESD element being bipolar transistor, thyristor or a diode in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3, 8, 10, 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 3, 8, 10, 12 and 13 depend on non-elected claims, thus rendering them indefinite. Note that if claim 1 is allowed, claims 3, 8, 10, 12 and 13 would not be allowed in their present format.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

7. Claims 1, 3, 8, 10, 12, 13, 21-23 and 25-29, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki et al. (4,456,939) in view of Miller (5,255,146), Puar (4,786,956) or Igarashi (4,656,491). Ozaki et al. teach in figure 2 a semiconductor device comprising a MOS capacitor 106 connected between a power source wire 107 and a ground potential wire, a power source terminal 103 to which voltage is applied, a ground terminal to which the ground potential wire is connected, and an ESD being a MOSFET connected in parallel with the capacitor, the drain of which is connected to the power source wire and the source and gate of which are connected to the ground potential wire.

Although Ozaki et al. do not state a MOS capacitor, MIS capacitor 106 includes a MOS capacitor, because it is conventional to form a gate dielectric comprising oxide, of which official notice is taken.

Ozaki et al. do not teach a wire resistance of the ground potential between the ESD element connection point and the ground terminal being larger than that between the ESD element connection point and the MOS capacitor's connection point.

A wire resistance is directly proportional to the length of the wire. Therefore, Ozaki et al. do not teach the layout design of the device, wherein the ground terminal being a distance from the ESD element connection point that is greater than the distance between the element connection point and the MOS capacitor's connection point. In

other words, Ozaki et al. do not teach the ESD protection circuit being located closer to the integrated circuit than to the ground pad.

Miller teaches in figure 2 ESD protection circuits 14 being located closer to the integrated circuit than to the ground pad 12a, such that the wire resistance of the ground potential between the ESD circuit connection point and the ground terminal is larger than the wire resistance between the ESD elements within the ESD circuit and the ground connection point.

Puar teaches in figure 1 an ESD protection circuit 16 being located closer to the integrated circuit 10 than to the ground pad (which is located beyond contact point 12), such that the wire resistance of the ground potential between the ESD circuit connection point and the ground terminal is larger than the wire resistance between the ESD elements within the ESD circuit and the ground connection point.

Igarashi teaches in figures 4-5 an ESD protection circuit being located closer to the integrated circuit than to the ground pad 103 (since wire 38 is connected to ground pad 103 away from figure 5, which depicts the ESD device), such that the wire resistance of the ground potential between the ESD circuit connection point and the ground terminal is larger than the wire resistance between the ESD elements within the ESD circuit and the ground connection point.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a circuit layout wherein the ground terminal being located a

distance from the ESD element connection point that is longer than the distance between the element connection point and the MOS capacitor's connection point in Ozaki et al.'s device, in order to simplify the processing steps of making the device by forming the ESD device with the integrated circuit away from the ground terminal, and in order to reduce the effect of noise associated with the ground terminal on the integrated circuit. Note that computer-aided design of integrated circuits is conventionally used nowadays to design semiconductor layouts, and it is well within the skills of an artisan to find the optimum layout of the device by routine experimentation and optimization.

Regarding claims 3 and 22, Ozaki et al. teach no other diffusion layer except the ESD element is connected on the ground potential wire between the ground terminal and the connection point on the ground potential wire with one end of the MOS capacitor.

Regarding claims 10 and 25, although Ozaki et al. do not explicitly disclose the ESD element clamps a voltage applied to both terminals at a clamp voltage which is lower than the dielectric breakdown voltage of the MOS capacitor, this feature is inherent in Ozaki et al.'s device, because Ozaki et al.'s structure is identical to the claimed structure.

Regarding claims 27-29, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an ESD element comprising bipolar transistor, thyristor or a diode in Ozaki et al.'s device, in order to use the device in an application which requires such ESD protection.

Response to Arguments

8. Applicant argues on page 4 that the subject matter of claim 24 is supported by the elected species, and is discussed on page 18, lines 20-23.

The subject matter of claim 24 is discussed on page 18, lines 20-23, but it is not supported by the elected species. The passage on page 18, lines 20-23 recites that the limitations of claim 24 are shown in figure 2. Applicant elected figure 1 for examination, and not figure 2. Therefore, the subject matter of claim 24 is not supported by the elected species.

9. Applicant argues on pages 5-7 that the examiner did not detail why an artisan would not understand how to use a bipolar transistor, a thyristor or a diode as an ESD element in the embodiment of figure 1. Applicant further argues that the subject matter of claim 24 is supported by the embodiments of figures 9-14.

Applicant admits that the use of a bipolar transistor, a thyristor or a diode as an ESD element is described in the embodiments of figures 4-14 (page 6 of applicant's arguments). Applicant elected the embodiment of figure 1 for examination. Therefore, there is no adequate description in the disclosure of the embodiment of figure 1 for an ESD element being bipolar transistor, thyristor or a diode.

10. Applicant argues on page 9 that there is no evidence that optimum layout of a device is done by using computers.

The examiner cited Cohn in previous office action to support the well known position that optimum layout of a device is done by using computers (column 1, lines 11-19).

11. Applicant argues on pages 9-14 that there is no motivation to combine Ozaki et al. and Miller, Puar or Igarashi.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re*

Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it is well known in the semiconductor industry that noise is associated with ground terminals. Thus, forming semiconductor circuits, including ESD devices away from the ground terminal, would reduce the effect of noise associated with the ground terminal. Furthermore, computer-aided design tools of integrated circuits is conventionally used nowadays to design semiconductor layouts, and it is well within the skills of an artisan to find the optimum layout of the device.

12. Applicant argues on page 14 that Igarashi teaches in figures 4 and 5 the opposite of the claimed resistive relationship, because resistor R12 is connected between transistors Q11 and Q1n, and very little resistance is present between the ground terminal and transistor Q1n.

The examiner did not cite Igarashi to teach the claimed resistive relationship. The examiner cited Igarashi to teach an artisan that an ESD protection circuit is located closer to the integrated circuit than to the ground pad.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such

papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ori Nadav

August 22, 2002